1. An apparatus for correcting time-gap defects in a computer system configured to communicate with devices of both synchronous and asynchronous types, the apparatus comprising:

a processor configured to process data communicated with devices of both synchronous and asynchronous types; and

a controller configured to control an exchange of data between the devices, the controller including a buffer, having a capacity of bytes and configured to temporarily store the data exchanged, and

a memory device operably connected to the processor to store data structures comprising executables, the executables comprising:

a driver configured to control operation of the controller, and

an error avoidance module, the error avoidance module configured to be invoked by the driver to compare the capacity to a count of bytes transferred with respect to the buffer, and to force an error condition based on the count.

2. The apparatus of claim 1, wherein the error condition is forced if the value of the count is at least as large as the capacity.

3. The apparatus of claim 1, wherein the error condition is forced if the value of the count is at least as large as the capacity of the buffer added to a value corresponding to bytes that have been transferred both into and out of the buffer during a transfer operation between the buffer and the processor.

4. The apparatus of claim 1, wherein the driver further comprises an initialization module configured to enable the error avoidance module.

5. The apparatus of claim 4, wherein the initialization module is further configured to enable a content-limiting interrupt configured to occur when the content of the buffer approaches a capacity limit.

6. The apparatus of claim 5, wherein the capacity limit comprises a plurality of limits.

7. The apparatus of claim 5, wherein the capacity limit is selected from the group consisting of a high and a low limit.

8. The apparatus of claim 5, wherein the capacity limit comprises both high and low limits.

9. The apparatus of claim 5, wherein the content-limiting interrupt is configured to trigger the execution of the error avoidance module.

10. The apparatus of claim 9, wherein the error avoidance module is configured to detect one of a read and a write operation.

11. The apparatus of claim 10, wherein the error avoidance module is configured to detect both a read and a write operation.

12. The apparatus of claim 11, wherein the buffer is selected from the group consisting of a register, a FIFO, and a content-addressable memory.

13. A method for correcting time-gap defects in a computer system configured to communicate with devices of both synchronous and asynchronous types, the method comprising:

transferring bytes of data between a device and a buffer having a capacity;

providing a count of the bytes;

comparing the count to the capacity; and

forcing an error condition based on the count.

14. The method of claim 13, wherein the error condition is forced if the value of the count is at least as large as the capacity.

15. The method of claim 13, wherein the error condition is forced if the value of the count is at least as large as the capacity of the buffer added to a value corresponding to bytes that have been transferred both into and out of the buffer during a transfer operation between the buffer and a processor.

16. The method of claim 13, further comprising enabling a content-limiting interrupt configured to occur when the content of the buffer approaches a capacity limit.

17. The method of claim 16, wherein the capacity limit is a plurality of limits.

18. The method of claim 16, wherein the capacity limit is selected from the group consisting of a high and a low limit.

19. The method of claim 16, wherein the capacity limit is both high and low limits.

20. The method of claim 16, wherein the content-limiting interrupt is configured to trigger to initialize the count.

21. The method of claim 20, wherein the buffer is selected from the group consisting of a register, a FIFO, and a content addressable memory.

22. An article including a computer readable medium configured to correct programmatic time-gap defects in a computer system having synchronous and asynchronous devices interconnected to one another, the apparatus comprising:

a controller driver configured to control operation of a controller in the computer system;

an error avoidance module configured to count the number of bytes transferred with respect to a buffer used by the controller, during an exchange of data, and to force an error condition based on the count.

23. The article of claim 22, wherein the controller driver further comprises an initialization module configured to enable the error avoidance module.

24. An apparatus for correcting programmatic time-gap defects, the apparatus comprising:

a processor configured to communicate with devices of both synchronous and asynchronous types; and

a controller for controlling an exchange of data between the devices, the controller including a buffer, having a byte capacity; and

a memory device configured to store executables comprising:

a driver configured to control the controller and invoke an error avoidance module, and

the error avoidance module configured to compare the byte capacity to a count of bytes transferred with respect to the buffer, and to force an error condition based on the count.